PRELIMINARY

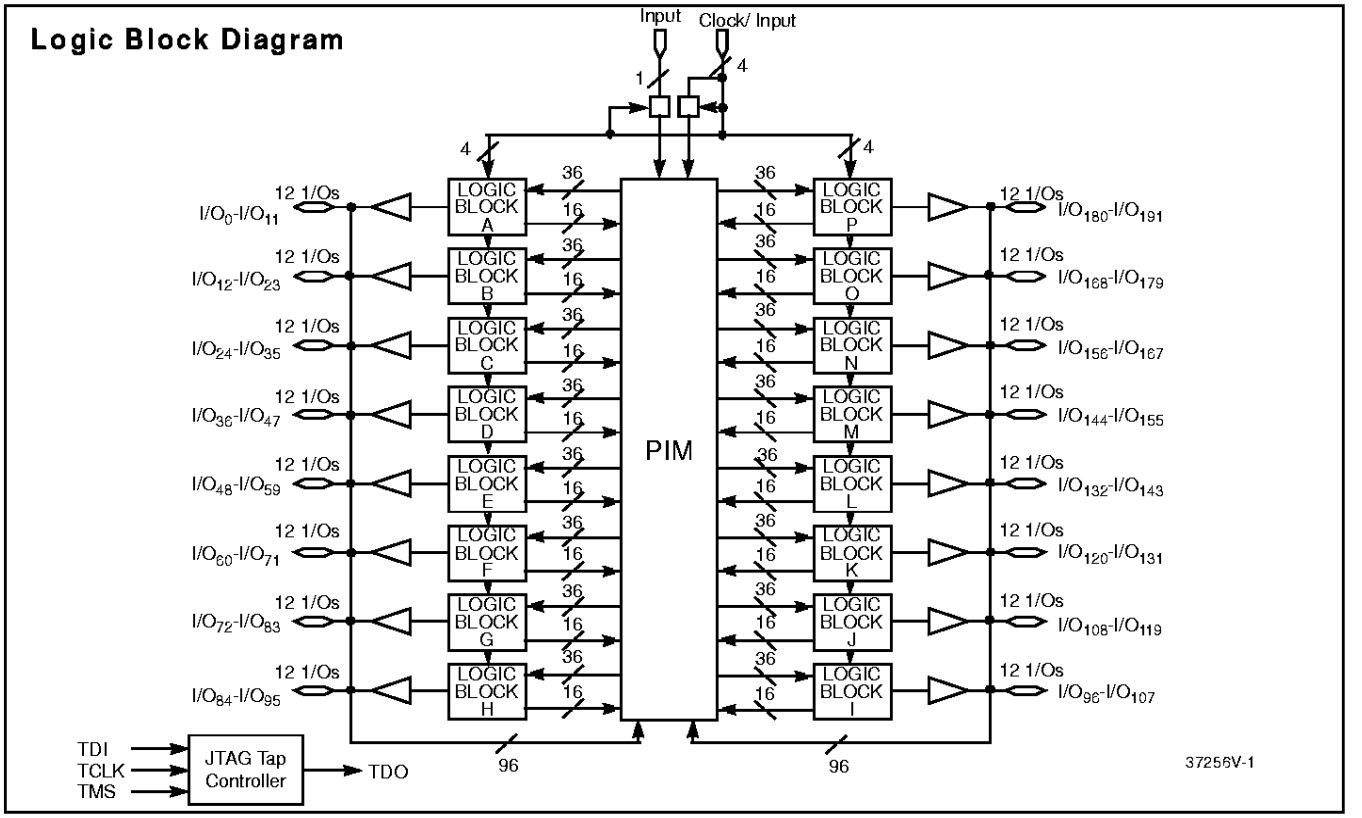
Ultra37256V

UltraLogic™ 256-Macrocell 3.3V ISR™ CPLD

Features

- 256 macrocells in sixteen logic blocks
- IEEE standard 3.3V operation
  - 3.3V ISR
  - 5V tolerant
- 3.3V In-System Reprogrammable (ISR™)
  - JTAG compliant on board programming
  - Design changes don't cause pinout changes
  - Design changes don't cause timing changes
- High speed
  - f_{MAX} = 125 MHz
  - t_{PD} = 10 ns
  - t_S = 5.5 ns
  - t_{CO} = 6.5 ns
- Up to 192 I/Os
  - plus 5 dedicated inputs including 4 clock inputs
- Product-term clocking
- IEEE1149.1 JTAG boundary scan
- Programmable slew rate control on individual I/Os
- Low power option on individual logic block basis
- Bus Hold capabilities on all I/Os
- Simple Timing Model
- Fully PCI compliant[1]
- Available in 160-pin TQFP, 208-pin PQFP and 256-lead BGA packages
- Pinout compatible with all other Ultra37000 family CPLDs

Logic Block Diagram



Selection Guide

	Ultra37256V-125	Ultra37256V-83
Maximum Propagation Delay, t_{PD} (ns)	10	15
Minimum Set-Up, t_S (ns)	5.5	8
Maximum Clock to Output, t_{CO} (ns)	6.5	8
Typical Supply Current, I_{CC} (mA) in Low Power Mode	120	120

Note:
1. Due to the 5-V tolerant nature of the I/Os, the I/Os are not clamped to Vcc.

Functional Description

The Ultra37256V is an In-System Reprogrammable (ISR) Complex Programmable Logic Device (CPLD) and is part of the Ultra37000™ family of high-density, high-speed CPLDs. Like all members of the Ultra37000 family, the Ultra37256V is designed to bring the ease of use and high performance of the 22V10 to high-density PLDs.

The 256 macrocell Ultra37256V is available in register intensive and I/O intensive versions. The Ultra37256VP160 features 96 Buried and 160 I/O Macrocells while the Ultra37256VP208 features 64 Buried Macrocells and 192 I/O Macrocells, for register intensive designs which require small footprint devices. The Ultra37256VP256 I/O intensive device has a I/O pin for each macrocell.

For a more detailed description of the architecture and features of the Ultra37256V see the Ultra37000 family data sheet.

Fully Routable with 100% Logic Utilization

The Ultra37256V is designed with a robust routing architecture which allows utilization of the entire device with a fixed pinout. This makes Ultra37000 optimal for implementing on board design changes using ISR without changing pinouts.

Simple Timing Model

The Ultra37256V features a very simple timing model with predictable delays. Unlike other high-density CPLD architectures, there are no hidden speed delays such as fanout effects, interconnect delays, or expander delays. The timing model allows for design changes with ISR without causing changes to system performance.

Low Power Operation

Each Logic Block of the Ultra37256V can be configured as either High-Speed (default) or Low-Power. In the Low-Power mode, the logic block consumes 50% less power (9.3 mA max.) and slows down by 6 ns.

Output Slew Rate Control

Each output can be configured with either a fast edge rate (default) for high performance, or a slow edge rate for added noise reduction. In the fast edge rate mode, outputs switch at 3V/ns max. and in the slow edge rate mode, Outputs switch at 1V/ns max. There is a 2-ns adder for I/Os using the slow edge rate mode.

In System Reprogramming

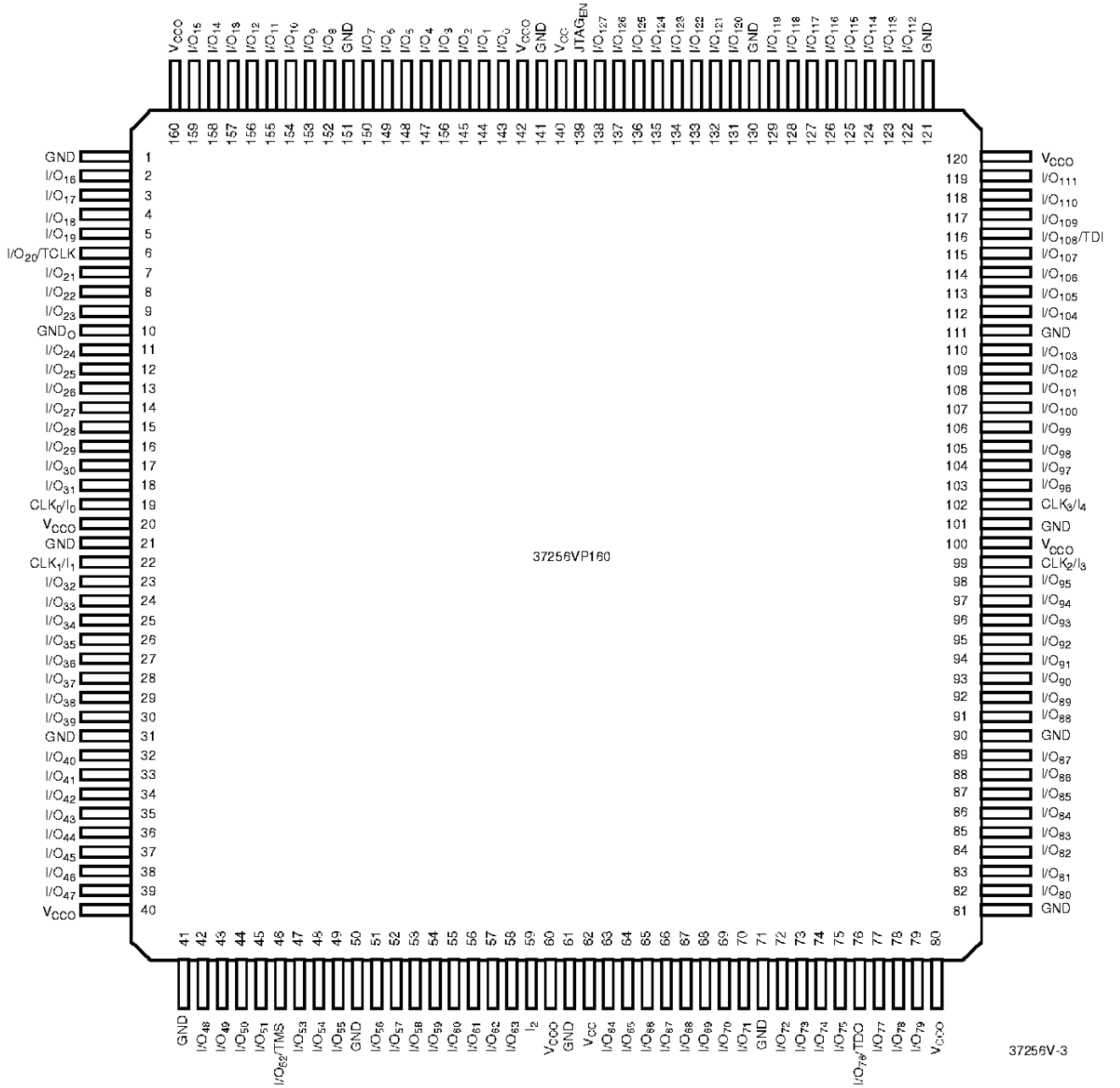
The Ultra37256V can be programmed in system using IEEE 1149.1 complaint JTAG programming protocol. The Ultra37256V can also be programmed on a number of traditional parallel programmers including Cypress's *Impulse3*™ programmer and industry standard third-party programmers. For an overview of ISR programming, refer to the Ultra37000 Family data sheet and for ISR cable and software specifications, refer to InSRkit: ISR programming data sheet (CY3600).

Design Tools

Development software for the Ultra37256V is available from Cypress's *Warp*™ or third-party bolt-in software packages as well as a number of third-party development packages. Please refer to the *Warp* or third-party tool support data sheets for further information.

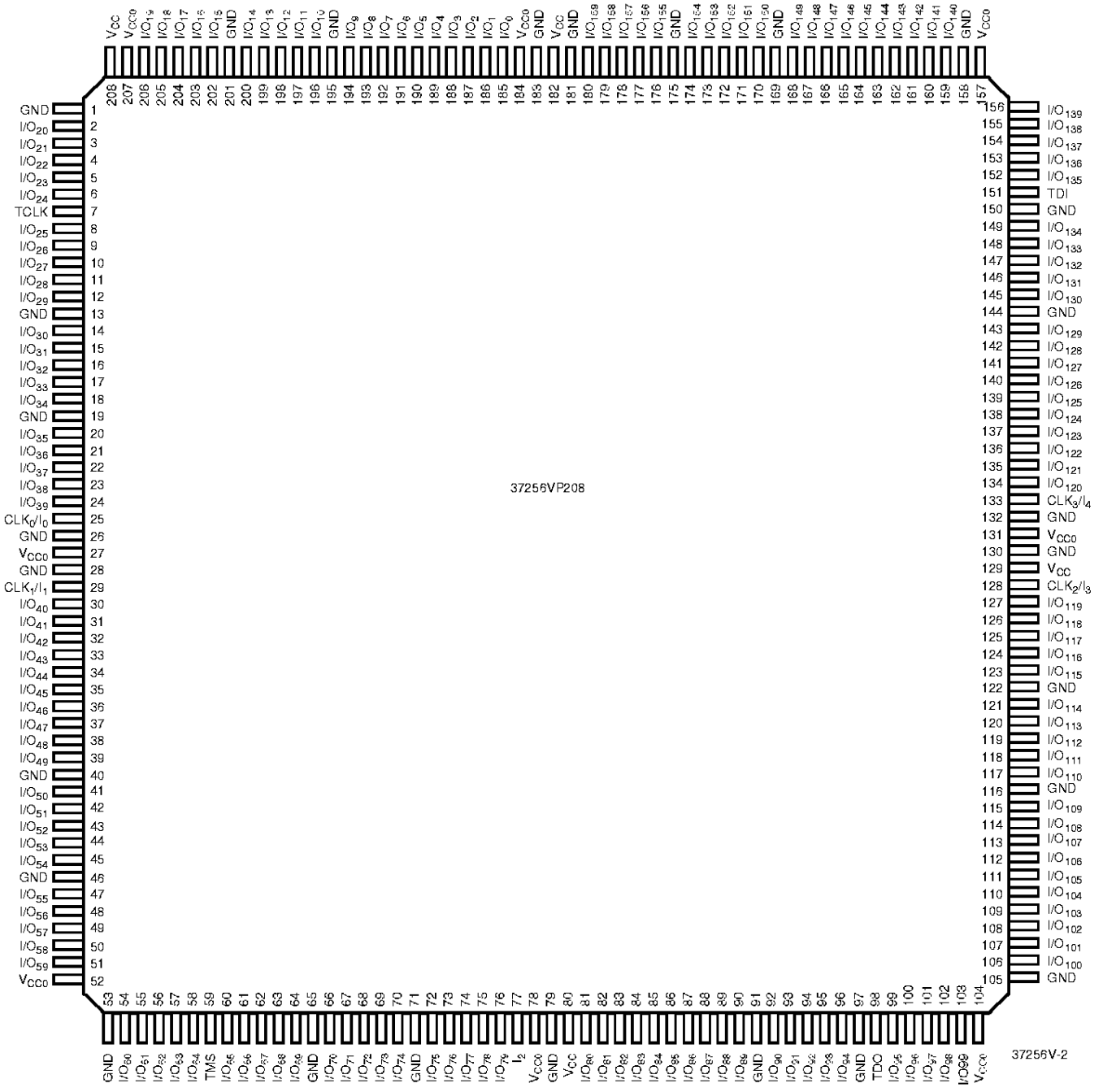
Pin Configurations

160-pin TQFP
Top View



Pin Configurations (continued)

208-pin PQFP
Top View



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage to Ground Potential..... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State..... –0.5V to +7.0V

DC Input Voltage..... –0.5V to +7.0V

DC Program Voltage..... 3.3V±0.3V

Output Current into Outputs ..... 8 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range[2]

Range	Ambient Temperature[2]	V_{CC}
Commercial	0°C to +70°C	3.3V ± 0.3V
Industrial	-40°C to +85°C	3.3V ± 0.3V
Military[3]	-55°C to +125°C	3.3V ± 0.3V

Shaded areas contain advance information.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –4 mA (Com'l)[4]	2.4		V
			I_{OH} = –3 mA (Mil)[4]			
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 8 mA (Com'l)[4]		0.5	V
			I_{OL} = 6 mA (Mil)[4]			
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH voltage for all inputs[5]		2.0	V_{CCmax}	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW voltage for all inputs[5]		–0.5	0.8	V
I_{IX}	Input Load Current	V_I = Internal GND, V_I = V_{CC}		–10	10	µA
I_{OZ}	Output Leakage Current	V_O = GND or V_{CC}, Output Disabled		–50	50	µA
I_{OS}	Output Short Circuit Current[6, 7]	V_{CC} = Max., V_{OUT} = 0.5V		–30	–160	mA
$I_{CC\text{-}HS}$	Power Supply Current[8] Per Logic Block - High Speed Mode	V_{CC} = Max., I_{OUT} = 0 mA,f = 1 MHz, V_{IN} = GND or V_{CC}			18.7	mA
$I_{CC\text{-}LP}$	Power Supply Current[8] Per Logic Block - Low Power Mode	V_{CC} = Max., I_{OUT} = 0 mA,f = 1 MHz, V_{IN} = GND or V_{CC}			9.3	mA
I_{BHL}	Input Bus Hold LOW Sustaining Current	V_{CC} = Min., V_{IL} = 0.8V		+75		µA
I_{BHH}	Input Bus Hold HIGH Sustaining Current	V_{CC} = Min., V_{IH} = 2.0V		–75		µA
I_{BHLO}	Input Bus Hold LOW Overdrive Current	V_{CC} = Max.			+500	µA
I_{BHHO}	Input Bus Hold HIGH Overdrive Current	V_{CC} = Max.			–500	µA

Inductance[7]

Parameter	Description	Test Conditions	160-lead TQFP	208-lead PQFP	Unit
L	Maximum Pin Inductance	V_{IN} = 3.3V at f = 1 MHz	9	11	nH

Note:

2. Normal Programming Conditions apply across Ambient Temperature Range for specified programming methods. For more information on programming the Ultra37000 family devices see the Ultra37000 family data sheet.
3. T_A is the "instant on" case temperature.
4. I_{OH} = –2 mA, I_{OL} = 2 mA for SDO.
5. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
6. Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
7. Tested initially and after any design or process changes that may affect these parameters.
8. Measured with 16-bit counter programmed into the logic block. Total device power calculated by summing the I_{CC} specifications for the mode of operation of each logic block.

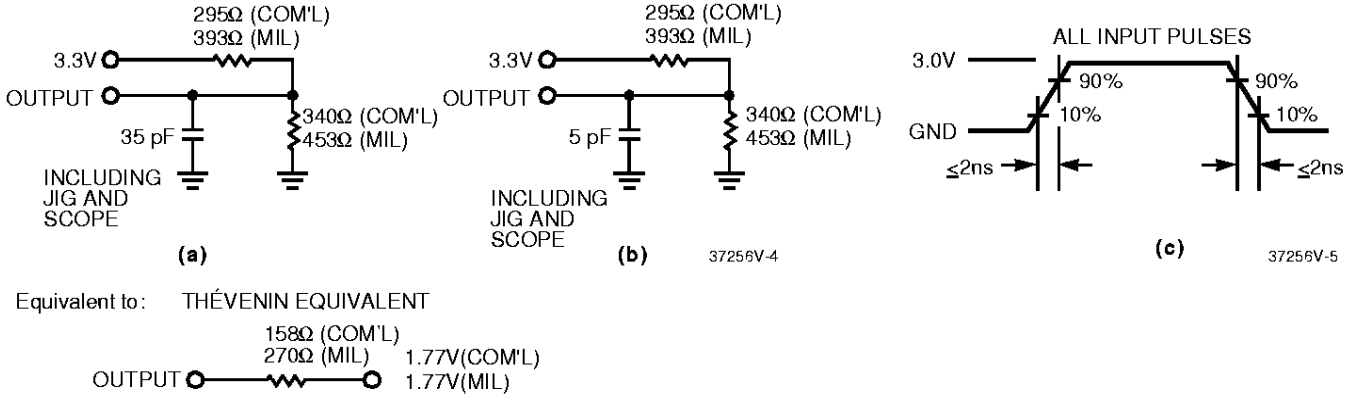
Capacitance[7]

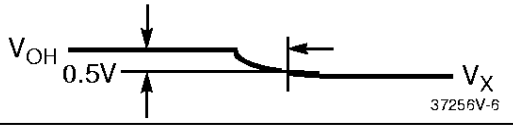
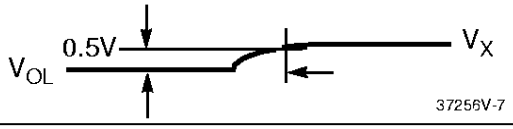
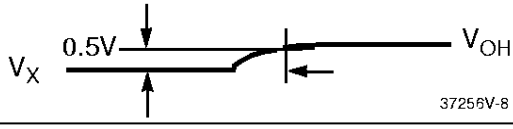
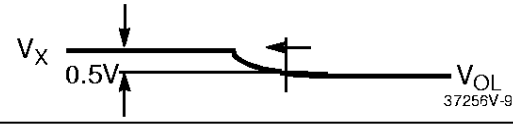
Parameter	Description	Test Conditions	Max.	Unit
$C_{I/O}$	Input/Output Capacitance	V_{IN} = 3.3V at f = 1 MHz	8	pF
C_{CLK}	Clock Signal Capacitance	V_{IN} = 3.3V at f = 1 MHz	12	pF

Endurance Characteristics[7]

Parameter	Description	Test Conditions	Min.	Typ.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions[2]	1,000	10,000	Cycles

AC Test Loads and Waveforms



Parameter[9]	V_X	Output Waveform--Measurement Level
$t_{ER(-)}$	1.5V	
$t_{ER(+)}$	2.6V	
$t_{EA(+)}$	1.5V	
$t_{EA(-)}$	V_{the}	

(d) Test Waveforms

Note:

9. t_{ER} measured with 5-pF AC Test Load and t_{EA} measured with 35-pF AC Test Load.

Switching Characteristics Over the Operating Range[10]

Parameter	Description	37256V-125		37256V-83		Unit
		Min.	Max.	Min.	Max.	
Combinatorial Mode Parameters						
t_{PD}[11]	Input to Combinatorial Output		10		15	ns
t_{PDL}[11]	Input to Output Through Transparent Input or Output Latch		13		18	ns
t_{PDLL}[11]	Input to Output Through Transparent Input and Output Latches		15		19	ns
t_{EA}[12]	Input to Output Enable		14		19	ns
t_{ER}	Input to Output Disable		14		19	ns
Input Register Parameters						
t_{WL}	Clock or Latch Enable Input LOW Time[7]	3		4		ns
t_{WH}	Clock or Latch Enable Input HIGH Time[7]	3		4		ns
t_{IS}	Input Register or Latch Set-Up Time	2		3		ns
t_{IH}	Input Register or Latch Hold Time	2		3		ns
t_{ICO}[11]	Input Register Clock or Latch Enable to Combinatorial Output		14		19	ns
t_{ICOL}[11]	Input Register Clock or Latch Enable to Output Through Transparent Output Latch		16		21	ns
Synchronous Clocking Parameters						
t_{CO}[12]	Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable to Output		6.5		8	ns
t_S[11]	Set-Up Time from Input to Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable	5.5		8		ns
t_H	Register or Latch Data Hold Time	0		0		ns
t_{CO2}[11, 12]	Output Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable to Combinatorial Output Delay (Through Logic Array)		14		19	ns
t_{SCS}[11]	Output Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable to Output Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable (Through Logic Array)	8		12		ns
t_{SL}[11]	Set-Up Time from Input Through Transparent Latch to Output Register Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable	10		15		ns
t_{HL}	Hold Time for Input Through Transparent Latch from Output Register Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable	0		0		ns
Product Term Clocking Parameters						
t_{COPT}[11, 12]	Product Term Clock or Latch Enable (PTCLK) to Output		12		17	ns
t_{SPT}[11]	Set-Up Time from Input to Product Term Clock or Latch Enable (PTCLK)	3		3		ns
t_{HPT}	Register or Latch Data Hold Time	3		3		ns
t_{ISPT}[11]	Set-Up Time for buried register used as an input register from Input to Product Term Clock or Latch Enable (PTCLK)		–2		–2	ns
t_{IHPT}	Buried Register used as an input register or Latch Data Hold Time		9		14	ns
t_{CO2PT}[11, 12]	Product Term Clock or Latch Enable (PTCLK) to Output Delay (Through Logic Array)		16		21	ns

Switching Characteristics Over the Operating Range[10] (continued)

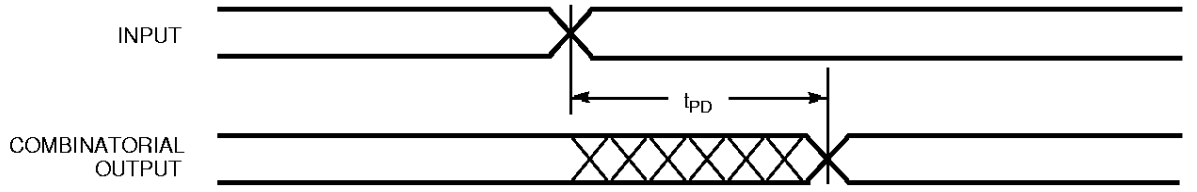
Parameter	Description	37256V-125		37256V-83		Unit
		Min.	Max.	Min.	Max.	
Pipelined Mode Parameters						
t_{ICS}[11, 12]	Input Register Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) to Output Register Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3)	8		12		ns
Operating Frequency Parameters						
f_{MAX1}	Maximum Frequency with Internal Feedback (Least of $1/t_{SCS}$, $1/(t_S + t_H)$, or $1/t_{CO}$)[7]	125		83		MHz
f_{MAX2}	Maximum Frequency Data Path in Output Registered/Latched Mode (Lesser of $1/(t_{WL} + t_{WH})$, $1/(t_S + t_H)$, or $1/t_{CO}$)	153.8		125		MHz
f_{MAX3}	Maximum Frequency with External Feedback (Lesser of $1/(t_{CO} + t_S)$ or $1/(t_{WL} + t_{WH})$)	83.3		62.5		MHz
f_{MAX4}	Maximum Frequency in Pipelined Mode (Least of $1/(t_{CO} + t_{IS})$, $1/t_{ICS}$, $1/(t_{WL} + t_{WH})$, $1/(t_{IS} + t_{IH})$, or $1/t_{SCS}$)	125		66.6		MHz
Reset/Preset Parameters						
t_{RW}	Asynchronous Reset Width[7]	10		15		ns
t_{RR}	Asynchronous Reset Recovery Time[7]	12		17		ns
t_{RO}[11, 12]	Asynchronous Reset to Output		16		21	ns
t_{PW}	Asynchronous Preset Width[7]	10		15		ns
t_{PR}	Asynchronous Preset Recovery Time[7]	12		17		ns
t_{PO}[11, 12]	Asynchronous Preset to Output		16		21	ns
User Option Parameters						
t_{LP}	Low Power Adder	6		6		ns
t_{SLEW}	Slow Output Slew Rate Adder	2		2		ns
Tap Controller Parameter						
f_{TAP}	Tap Controller Frequency		20		20	MHz

Notes:

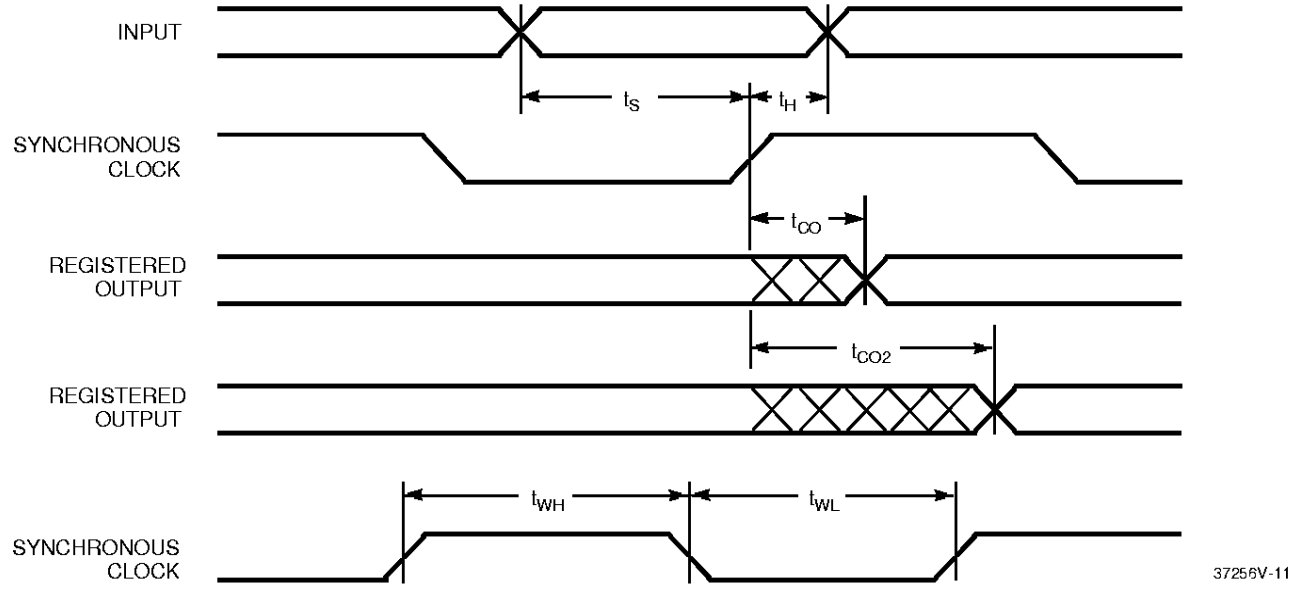
10. All AC parameters are measured with 16 outputs switching and 35-pF AC Test Load.
11. Logic Blocks operating in low power mode, add t_{LP} to this spec.
12. Outputs using Slow Output Slew Rate, add t_{SLEW} to this spec.

Switching Waveforms

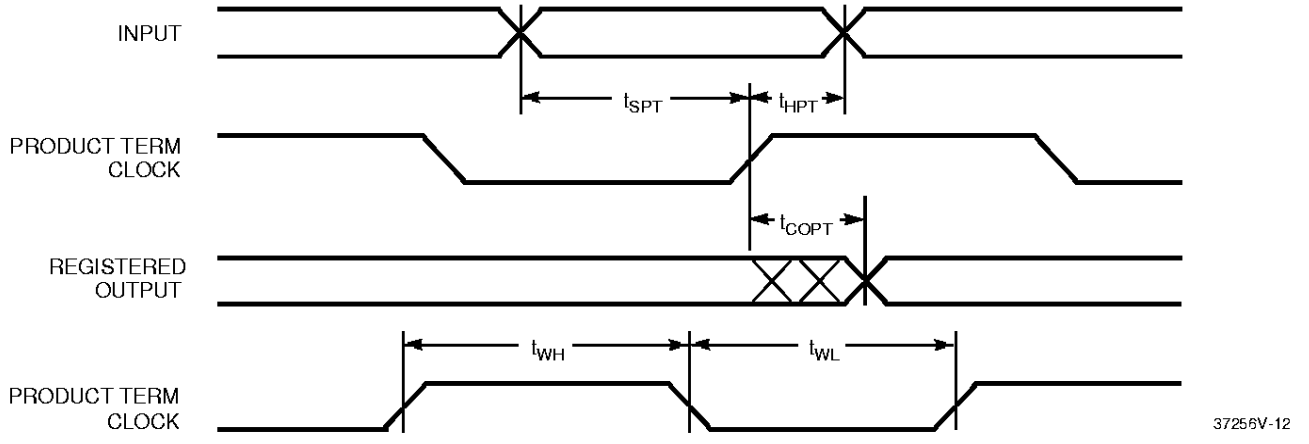
Combinatorial Output



Registered Output with Synchronous Clocking

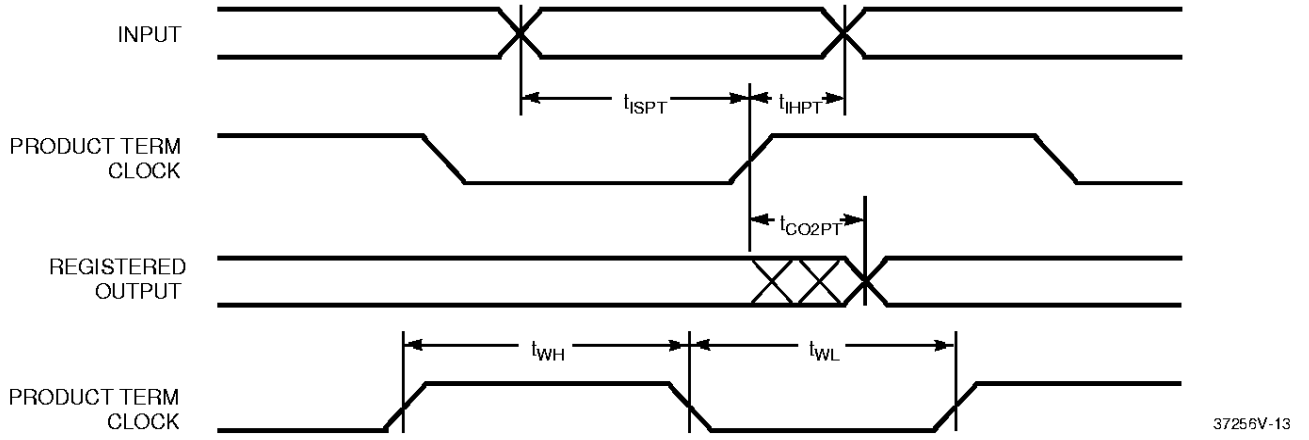


Registered Output with Product Term Clocking Input going through the Array



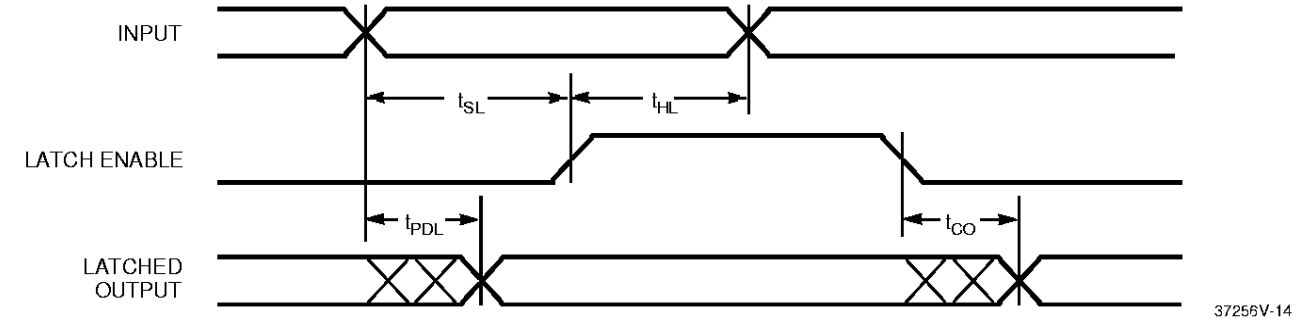
Switching Waveforms (continued)

Registered Output with Product Term Clocking Input coming from Adjacent Buried Register



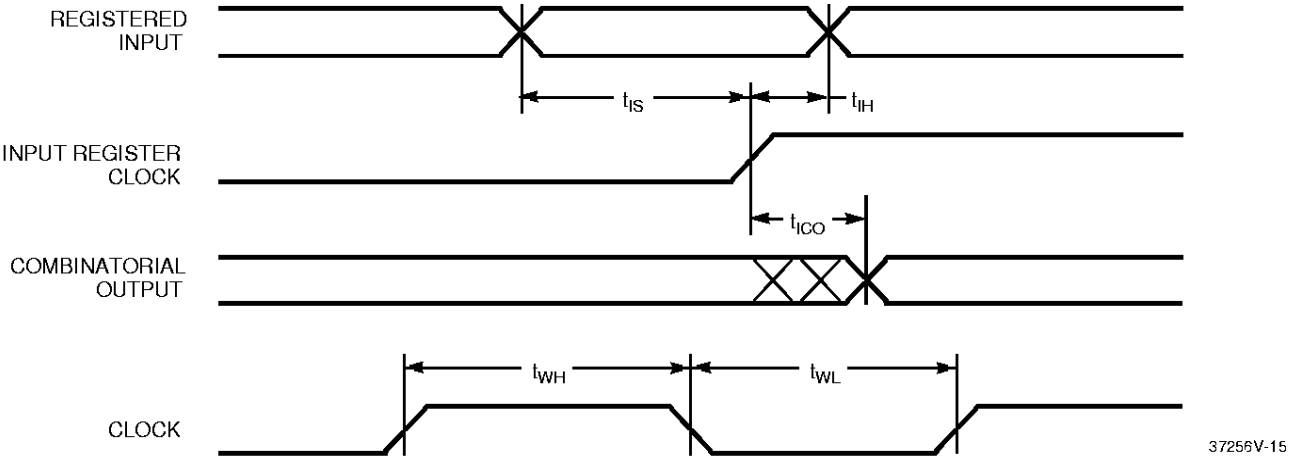
37256V-13

Latched Output



37256V-14

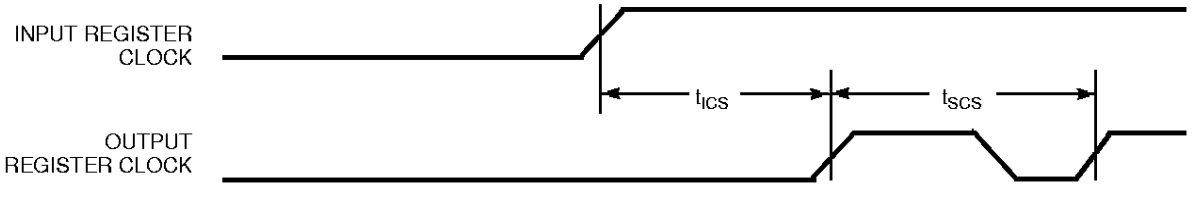
Registered Input



37256V-15

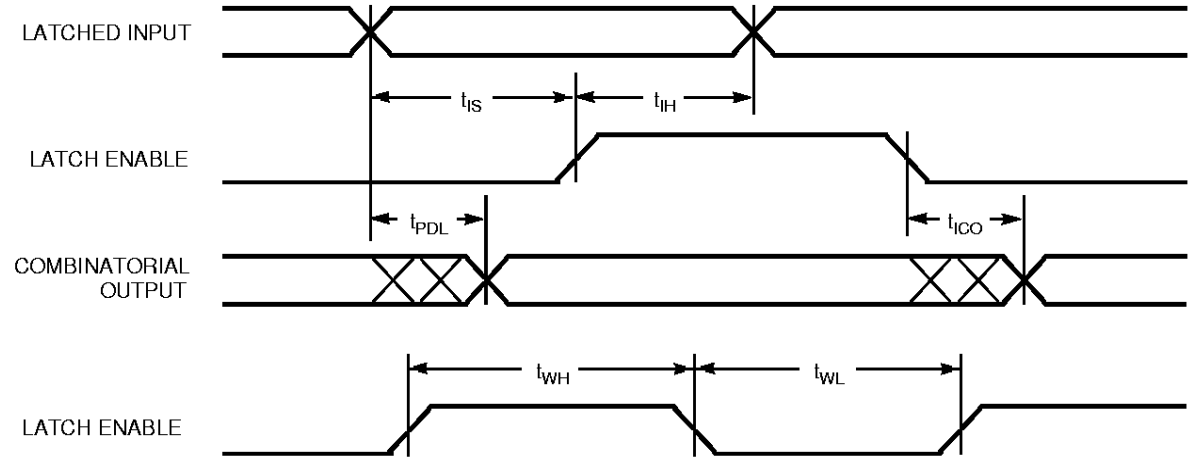
Switching Waveforms (continued)

Clock to Clock



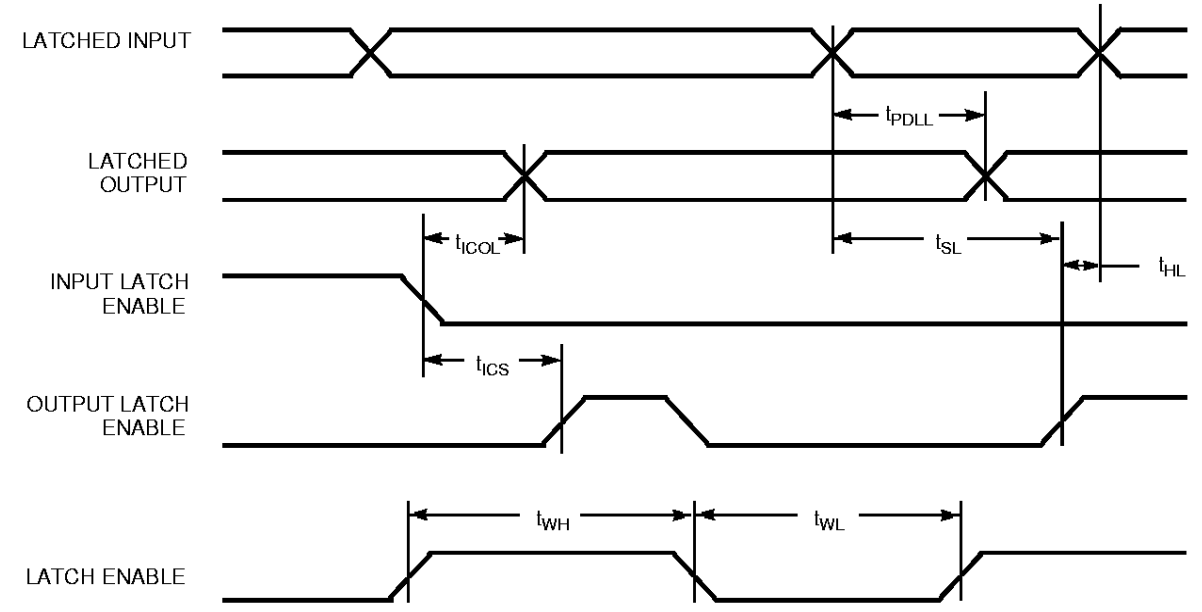
37256V-16

Latched Input



37256V-17

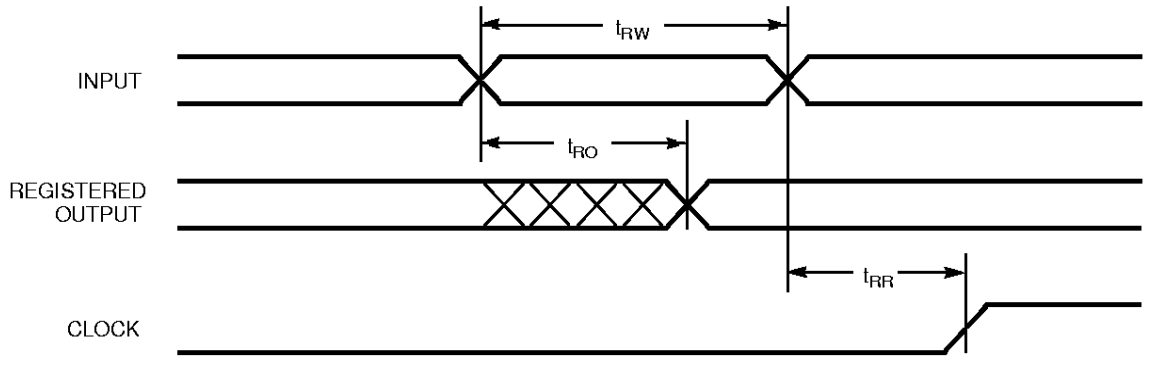
Latched Input and Output



37256V-18

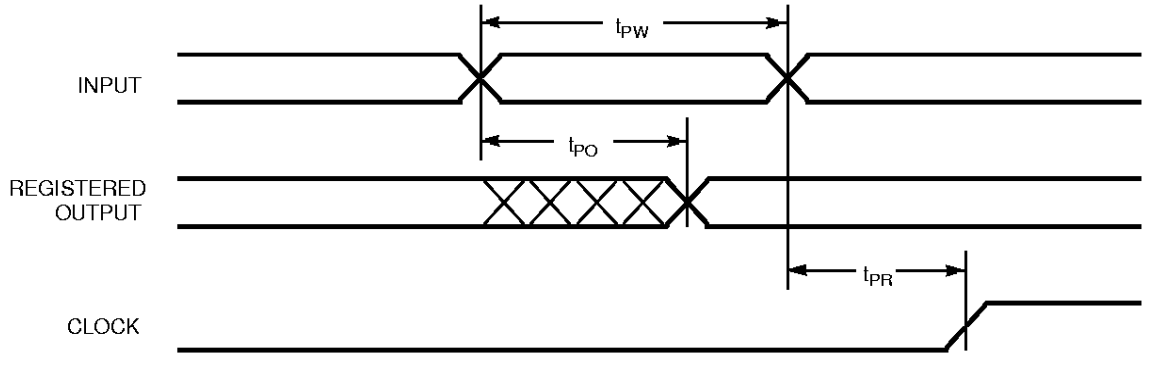
Switching Waveforms (continued)

Asynchronous Reset



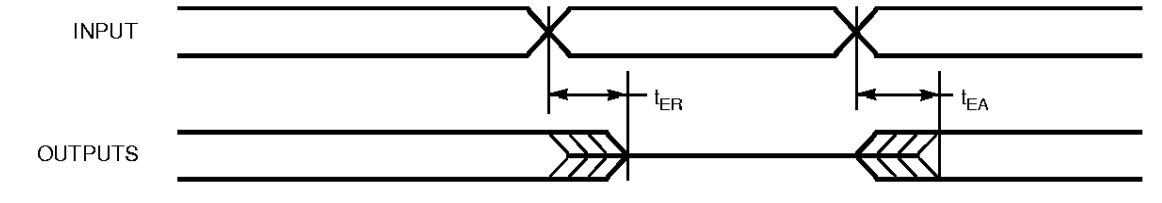
37256V-19

Asynchronous Preset



37256V-20

Output Enable/Disable



37256V–21

Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
125	CY37256VP160–125AC	A160	160-Pin Thin Quad Flatpack	Commercial
	CY37256VP208-125NC	N208	208-Pin Plastic Quad Flatpack	
	CY37256VP256-125BGC	BG256	256-Lead Ball Grid Array	
	CY37256VP160–125AI	A160	160-Pin Thin Quad Flatpack	Industrial
	CY37256VP208-125NI	N208	208-Pin Plastic Quad Flatpack	
83	CY37256VP160–83AC	A160	160-Pin Thin Quad Flatpack	Commercial
	CY37256VP208-83NC	N208	208-Pin Plastic Quad Flatpack	
	CY37256VP256-83BGC	BG256	256-Lead Ball Grid Array	
	CY37256VP160–83AI	A160	160-Pin Thin Quad Flatpack	Industrial
	CY37256VP208-83NI	N208	208-Pin Plastic Quad Flatpack	

Shaded areas contain advance information.

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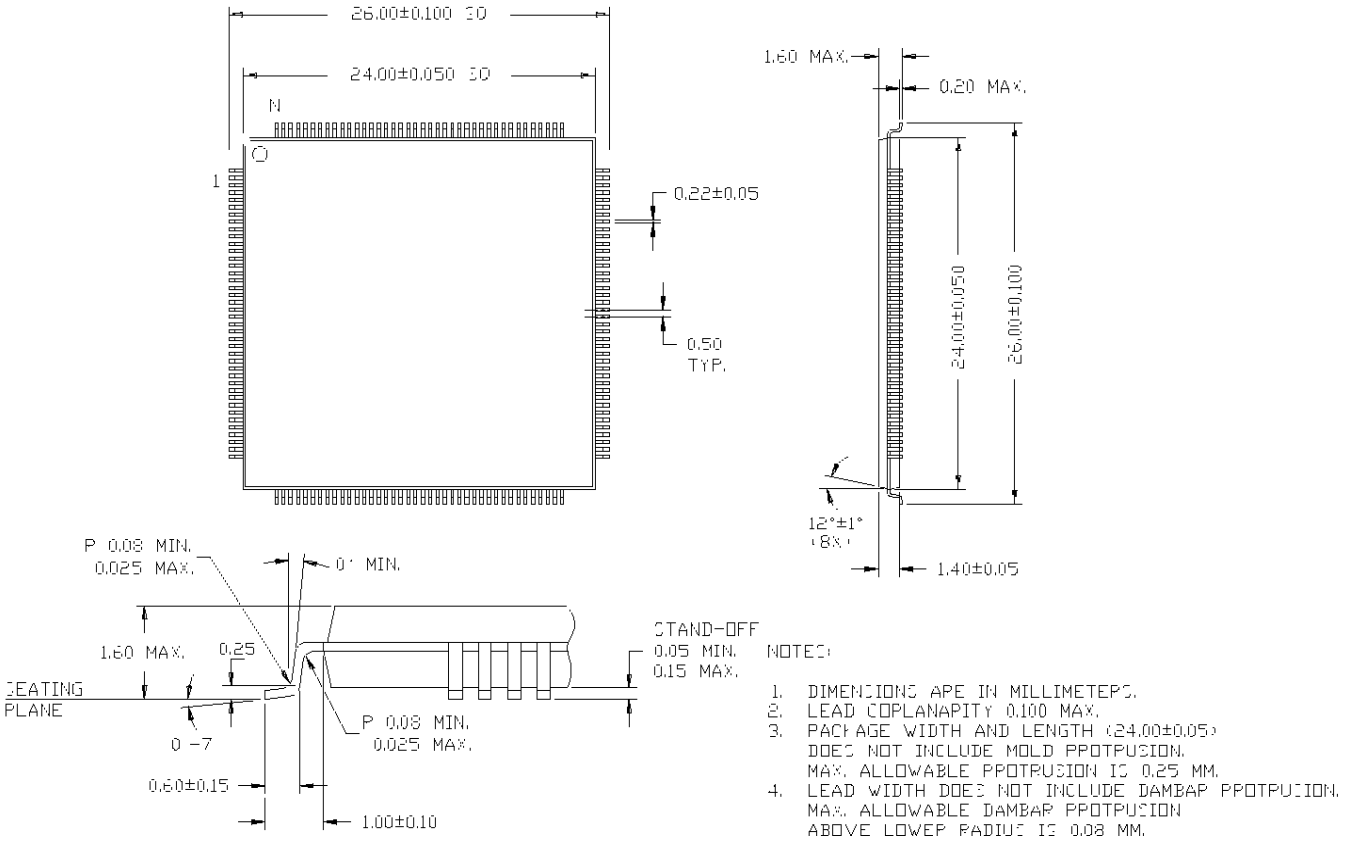
Package Diagrams

160-Lead Thin Quad Flat Pack (TQFP) A160



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. LEAD COPLANARITY 0.100 MAX.
3. PACKAGE WIDTH AND LENGTH (24.00±0.05) DOES NOT INCLUDE MOLD PROTRUSION. MAX. ALLOWABLE PROTRUSION IS 0.25 MM.
4. LEAD WIDTH DOES NOT INCLUDE DAMBAR PROTRUSION. MAX. ALLOWABLE DAMBAR PROTRUSION ABOVE LOWER RADIUS IS 0.08 MM.

Package Diagrams (continued)

208-Lead Plastic Quad Flatpack N208